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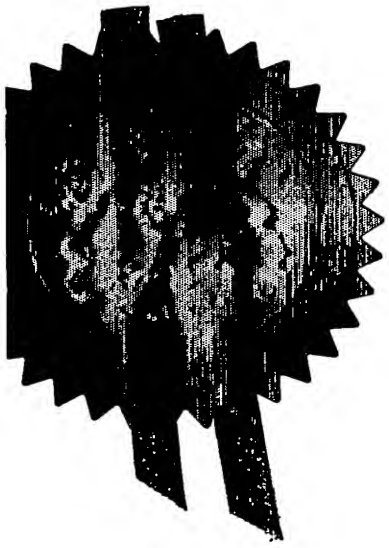

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04AUG03 E827365-1 D00354
P01/7700 0.00-0318146.8

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Request for grant of a patent

(see the notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)

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1.	Your reference	MH/P089452GB
2.	Patent application number *(The Patent Office will fill in this part)*	0318146.8 - 2 AUG 2003
3.	Full name, address and postcode of the or of each applicant *(underline all surnames)*	ZETEX PLC FIELDS NEW ROAD CHADDERTON OLDHAM OL9 8NP
	Patents ADP number *(if you know it)*	06199001
	If the applicant is a corporate body, give the country/state of its incorporation	UNITED KINGDOM
4.	Title of the invention	BIPOLAR TRANSISTOR WITH A LOW SATURATION VOLTAGE
5.	Name of your agent *(if you have one)*	Marks & Clerk
	"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*	Sussex House 83-85 Mosley Street Manchester M2 3LG
	Patents ADP number *(if you know it)*	18004

6.	If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number	Country	Priority application number *(if you know it)*	Date of filing *(day/month/year)*
7.	If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application		Number of earlier application	Date of filing *(day/month/year)*
8.	Is a statement of Inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:* *a) any applicant named in part 3 is not an inventor, or* *b) there is an inventor who is not named as an applicant, or* *c) any named applicant is a corporate body.* *See note (d))*	YES		

9. Enter the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document

Continuation sheets of this form	-
Description	7
Claim(s)	2 1 CF
Abstract	
Drawing(s)	1+1

10. If you are also filing any of the following, state how many against each item.

Priority documents	
Translations of priority documents	
Statement of Inventorship and right to grant of a patent *(Patents Form 7/77)*	
Request for preliminary examination and search *(Patents Form 9/77)*	1
Request for substantive examination *(Patents Form 10/77)*	
Any other documents *(Please specify)*	

11. I/We request the grant of a patent on the basis of this application.

Signature..... Date 1 August 2003
MARKS & CLERK

12. Name and daytime telephone number of person to contact in the United Kingdom MATTHEW HOLMES– 0161 233 5830

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Bipolar Transistor with a Low Saturation Voltage

The present invention relates to a bipolar transistor with a low saturation voltage.

With bipolar transistors, the collector-emitter saturation voltage is a key parameter determining the power loss of the transistor and its efficiency. In a circuit where the bipolar transistor is operated as a saturated switch a small base current is used to switch on a much larger collector to emitter current, the size of this current being determined by the voltage supply and the load resistance connected to either the collector or the emitter. When a bipolar transistor is operated in saturation the voltage drop from the collector to the emitter is reduced to a minimum value known as the saturation voltage $V_{CE(sat)}$. It is desirable to reduce this saturation voltage to as low a value as possible in order to minimise the power loss within the transistor.

There a number of known techniques to reduce the saturation voltage for a bipolar transistor, through either ensuring that the emitter / base junction is biased as evenly as possible across the whole junction area, or reducing the parasitic series resistance from the collector contact to the emitter contact.

In order to switch on the transistor a certain minimum voltage bias must be applied to the junction. If the junction is unevenly biased, then in some regions of the junction of the transistor will not be switched on, resulting in inefficient use of the silicon area. This increases the resistance of the transistor between the collector and the emitter when the transmitter is in the on state, resulting in a rise in the saturation voltage.

One known approach to address this problem is to provide frequent contacts to the base region through the emitter region to reduce the lateral resistance of the base layer extending under the emitter layer between these two points. A low lateral resistance is required so that the emitter / base bias voltage is not reduced in the centre of the emitter region remote from the base contact. However, it is desirable to achieve this effect without significantly affecting the percentage of the emitter / base

junction area left intact as this results in either a reduced emitter / base junction area or an enlarged transistor to maintain the same junction area.

Various approaches are known to reduce the lateral resistance of the base region such as creating striped contacts to the base region through the emitter region. However, this significantly reduces the area of the emitter / base junction with the disadvantages described above. A better approach is to provide an array of contacts to the base region through holes in the emitter region. These holes may typically be spaced less than 75μm apart, providing a good compromise between reducing the lateral resistance of the base region and maintaining the size of the emitter / base junction.

Reductions in the parasitic series resistance between the collector contact and the emitter contact of the transistor can be achieved in a number of ways. Using a low resistivity semiconductor (e.g. less than 5mOhm.cm) within the substrate reduces the resistance of the substrate. Additionally the thickness of the substrate and the epitaxial layers may be reduced. There is a trade off to be made when determining the thickness of the epitaxial collector layer as in the transistor off state this layer supports the widened depletion layer around the base / collector junction. The thinner the layer, the lower the transistor breakdown voltage will be. In the on state the depletion region collapses and the epitaxial layer represents just parasitic series resistance, proportional to its thickness, increasing the saturation voltage. An optimal epitaxial layer doping profile and thickness has to be obtained in order to achieve the optimal trade off between breakdown voltage performance and saturation voltage. The resistance of the wires connecting to the emitter, base and collector contact tracks can be reduced by using thick and / or multiple bond wires.

The current flow may be more evenly distributed and the voltage drops along the tracks reduced by altering the layout of the tracks. It is important to reduce the voltage drops in the tracks connecting to the emitter contacts as these directly contribute to the on resistance, reducing the saturation voltage.

Transistors incorporating some or all of the above techniques to reduce the saturation voltage are well known. The saturation voltage of a transistor can be

measured in terms of the specific area resistance of the transistor. The specific area resistance of a transistor is a well known term within the power semiconductor industry and refers to the product of the on resistance of the transistor (in the case of a bipolar transistor the collector to emitter resistance) multiplied by the area of the transistor. It is a figure of merit by which differing transistors may be compared, in respect of the on resistance and the area. The saturation voltage is equal to the on resistance of the transistor multiplied by the collector to emitter current.

Low $V_{CE(sat)}$ transistors with specific area resistances of below 500mOhm.mm^2 are now widely available. Nevertheless it remains desirable to find new ways of reducing the $V_{CE(sat)}$ of bipolar transistors. Accordingly it is an object of the present invention is to provide a new approach to reducing the specific area resistance and thus $V_{CE(sat)}$ of bipolar transistors.

According to the present invention there is provided a bipolar transistor, comprising:

a first semiconductor region of a first conductivity type defining a collector region;

a second semiconductor region of a second conductivity type defining a base region;

a third semiconductor region of said first conductivity type defining a emitter region; and

a metal layer providing contacts to said base and emitter regions;

wherein the transistor has a specific area resistance less than about 500mOhms.mm^2; and

wherein said metal layer has a thickness greater than about 3um.

The present inventors have recognised that in addition to reducing voltage drops in the metal tracks connecting to the emitter contacts, it is equally important to reduce the voltage drops in the metal tracks connecting to the base contacts as these serve to reduce the bias voltage applied to the emitter/base junction, potentially resulting in the junction being unevenly biased. The present inventors have shown that increasing the metal contact thickness of a low saturation voltage transistor in

accordance with the present invention can provide significant further reductions in saturation voltage. That is, with the present invention it is possible to achieve further reductions in the saturation voltage of a bipolar transistor above and beyond those reductions achieved through the application of prior art techniques as discussed above. This is achieved with minimal alteration to the design of the existing transistor, such that this approach may be applied to existing bipolar transistor designs with minimal alteration to the fabrication process, and hence minimal cost.

The present invention provides significant reductions in saturation voltage for bipolar transistors which would have a specific area resistance less than about 500mOhms.mm^2 with a conventional metal layer less than 3um thick. Improvements in saturation voltage may be even more marked with transistors having specific area resistances less than 300mOhms.mm^2. Additional reductions in saturation voltage of the order of 30% have been measured for transistors which would have a specific area resistance less about 200mOhms.mm^2 with a metal layer less than 3um thick.

It is preferable that the metal layer has a substantially uniform thickness greater than 3μm, or if not uniform has a minimum thickness greater than 3μm. Typically the metal layer will be less than 10μm thick.

In a preferred embodiment the emitter region defines a first surface, the base region extending to said surface in locations defined by apertures through emitter region, said metal layer overlying said first surface. The apertures are preferably spaced less than 100μm from each other.

Other objects and advantages of the present invention will become apparent from the following description.

A specific embodiment of the present invention will now be described, by way of example only, with reference to the accompanying drawing.

The illustrated bipolar transistor comprises a substrate 1, an epitaxial collector layer 2, a base region 3, emitter regions 4, oxide layer 5, base metal contacts 6 and emitter metal contacts 7.

The transistor is built upon a substrate 1 of a first conductivity type. An epitaxial layer 2 constituting the collector region of the first conductivity type is

grown upon the substrate 1. A base region 3 of a second and opposite conductivity type is formed into the epitaxial layer 2 and within the base region 3 areas of emitter regions 4 of the first conductivity type are formed. In the preferred embodiment of the present invention illustrated the emitter regions 4 are formed in a substantially continuous layer into the central portion of the base region 3, with the exception of an array of holes in the layer where no emitter doping takes place. The effect is that there is a regular array of circular holes in the emitter region 4 where the base region 3 extends to the surface of the emitter region 4. These holes are typically positioned approximately 75μm apart in a rectangular grid. Other patterns that ensure regular contact to the base region, without significantly reducing the area of the emitter region 4 / base region 3 junction are possible.

The drawing shows a cross sectional view of the bipolar transistor intersecting one row of this array of holes. The dashed line 8 indicates that remote from the holes where the base region 3 extends to the top of the emitter region 4 the coverage of the emitter region 4 is continuous over the base region 3. Over the top of the semiconductor layers a pattern of silicon oxide layer 5 is deposited and patterned bridging the upper edge of the boundary between the emitter region 4 and the base region 3. Interspersed between the oxide layer 5 are base metal contacts 6 and emitter metal contacts 7, separated from each other by the patterned oxide layer 5 and in electrical contact with the base region 6 and the emitter region 7 respectively. The collector connection is taken from the side of the substrate remote from the emitter regions.

As so far described, the bipolar transistor is entirely conventional and may be fabricated in an entirely conventional manner. However, in accordance with the present invention the metal layer contacts to the base and emitter regions are thicker than is conventional, i.e. greater than 3μm thick. Similarly, the emitter region metal layer contacts may be of an increased thickness.

The thickness of the metal layer defining the base contacts 6 and emitter contacts 7 is chosen in order to help ensure more even biasing of the emitter region 4/base region 3 junction to reduce the parasitic voltage drop across the emitter metal

contacts 7. Reducing the voltage drop in the tracks leading to the diverse base region contacts ensures that the voltage bias applied to the emitter / base junction is more evenly distributed, this ensures more even current density across the transistor, reducing the saturation resistance.

The inventors of the present invention have demonstrated that this seemingly simple expedient, when applied to a bipolar transistor already designed to have a low $V_{CE(sat)}$ (i.e. a specific area resistance less than about 500mOhms.mm^2, can provided further reductions in $V_{CE(sat)}$ of up to around 30%.

A bipolar transistor in accordance with the present invention will typically incorporate the prior art techniques described above to minimise the saturation voltage. In the specific embodiment, the array of contacts to the base region is designed to help ensure that the emitter / base junction remains evenly biased, low resistivity thin substrates are utilised and the epitaxial layer thickness and doping profile are chosen to reduce the resistance in the transistor on state. Additionally, the layout of the metal tracks is designed to help reduce the voltage drop along their lengths and the wire bonds to the tracks are constructed using thick and / or multiple wires. The effect is such that the saturation voltage of the bipolar transistor is reduced below the level achievable by the prior art alone.

A bipolar transistor not already optimised for low saturation voltage (i.e. with a specific area resistance greater than about 500mOhms.mm^2) would show no significant improvement to the saturation voltage by thickening the metal contact in accordance with the present invention since the saturation voltage is affected more by the other parameters described above than by the thickness of the metal contacts. With bipolar transistor designs already optimised for low saturation voltage increasing the thickness of the metal contacts further reduces the saturation voltage. This reduction in saturation voltage is progressive and proportional to the thickness of the metal contact and track. Significant improvements to the saturation voltage have been observed with a metal thickness of between 4μm and 6μm, with 6μm, the preferable thickness, reducing the saturation voltage of a bipolar transistor optimised for low saturation performance by a up to a further 30%.

It will be appreciated that the present invention is described in connection with a specific vertical bipolar transistor, optimised for low saturation voltage through existing known techniques. Thicker metal layers may be applied to any bipolar transistor design where it is desirable to reduce the voltage drop in the metal contact tracks in order to ensure more even biasing of the emitter / base junction.

The present invention offers improved performance for any power switching application where the circuit efficiency is dependent on the saturation voltage. Effectively this extends to all applications where the transistor is used in saturation rather than as a linear switch.

Further possible modifications and applications of the present invention will be readily apparent to the appropriate skilled person.

CLAIMS

1. A bipolar transistor, comprising:

a first semiconductor region of a first conductivity type defining a collector region;

a second semiconductor region of a second conductivity type defining a base region;

a third semiconductor region of said first conductivity type defining a emitter region; and

a metal layer providing contacts to said base and emitter regions;

wherein the transistor has a specific area resistance less than about 500mOhms.mm^2; and

wherein said metal layer has a thickness greater than about 3μm.

2. A bipolar transistor according to claim 1, wherein the metal layer has a thickness no less than 4μm.

3. A bipolar transistor according to any preceding claim, wherein the metal layer has a thickness no less than 6μm.

4. A bipolar transistor according to any preceding claim, wherein the emitter region defines a first surface, the base region extending to said surface in locations defined by apertures through emitter region, said metal layer overlying said first surface.

5. A bipolar transistor according to claim 4, wherein adjacent apertures are spaced less than 100μm from each other.

6. A bipolar transistor substantially as hereinbefore defined, with reference to the accompanying drawing.

Fig 1